What is claimed is:

1. A digital delay locked loop comprising:

a coarse delay segment to apply a coarse delay to an external clock signal to generate a coarse delayed signal;

a fine delay segment connected to the coarse delay segment to apply a fine delay to the coarse delayed signal to generate an internal clock signal; and

wherein the fine delay segment is capable of adjusting the fine delay based on shifting signals that are generated when the external and internal signals are not synchronized, wherein the coarse delay capable of adjusting the coarse delay based on the shifting signals and the fine delay applied to the coarse delay signal.

2. The DLL of claim 1, wherein the coarse delay is within a coarse delay range of the coarse delay segment, wherein the fine delay is within a fine delay range of the fine delay segment, and wherein the fine delay range is smaller than the coarse delay range.

3. The DLL of claim 1, wherein the coarse delay is within a coarse delay range of the coarse delay segment, wherein the fine delay is within a fine delay range of the fine delay segment, wherein a largest delay of the fine delay range is smaller than a smallest delay of a coarse delay range.

4. The DLL of claim 1, wherein the coarse delay segment adjusts the coarse delay only when the fine delay segment applies a minimum delay of a fine delay range of the fine delay segment and the shifting signals indicate a decrease in the delay is necessary.

5. The DLL of claim 1, wherein the coarse delay segment adjusts the coarse delay only when the fine delay segment applies a maximum delay of the fine delay range and the shifting signals indicate an increase in the delay is necessary.

6. The DLL of claim 1, wherein each time the coarse delay segment adjusts the coarse delay, the fine delay segment changes the fine delay to a different delay within a delay range of the fine delay segment.

7. A digital delay locked loop comprising:

a coarse delay segment to apply a coarse delay to an external clock signal to generate a coarse delayed signal;

a fine delay segment connected to the coarse delay segment to apply a number of unequal amounts of fine delay to the coarse delayed signal to generate a plurality of fine delayed signals having different phase shifts,

a phase detector to generate shifting signals based on a difference in phase between the external and internal clock signals, wherein based on the shifting signals, the fine delay segment selects one of the fine delay signals to provide an internal clock signal; and

a logic circuit to receive the shifting signals and the select signal to enable the coarse delay segment to adjust the coarse delay.

8. The DLL of claim 7, wherein each time the coarse delay segment adjusts the coarse delay, the fine delay segment switches the internal clock signal between a fine delayed signal having a minimum amount of delay and a fine delayed signal having maximum amount of delay within a fine delay range.

9. The DLL of claim 7, wherein each time the coarse delay segment adjusts the coarse delay, the fine delay segment switches the internal clock signal between

two fine delayed signals having unequal amounts of delay within a fine delay range.

10. The DLL of claim 7, wherein the coarse segment includes:

a delay line including a plurality of delay stages to apply the coarse delay to the external clock signal, each of the delay stages includes a delay time; and

a controller connected to the logic circuit and the delay line, the controller causing the delay line to adjust the coarse delay based on the shifting signals and the select signal.

11. The DLL of claim 10, wherein the fine delay segment includes:

a plurality of fine delay paths to receive the coarse delayed signal to provide the plurality of fine delay signals, each of the fine delay paths includes a delay time;

a selector connected to the delay paths to receive the fine delay signals; and

a shift register connected to the phase detector and the selector, the shift register receiving the shifting signals to activate the select signal, wherein the selector selects one of the fine delay signals based on the activated select signal to generate the internal clock signal.

12. The DLL of claim 11, wherein the delay time of each of the delay stages of the coarse delay segment is greater than the delay time of each of the fine delay paths.

13. A delay locked loop comprising:

a coarse delay line to apply a coarse delay to an external clock signal to generate a coarse delayed signal;

a plurality of fine delay paths connected to the coarse delay line to apply unequal amounts of fine delay to the coarse delayed signal to generate a plurality of fine delayed signals;

a selector connected to the fine delay paths to select one of the fine delayed signals based on select signals to provide an internal clock signal;

a phase detector to compare the external and internal clock signals to provide shifting signals;

a shift register connected to the phase detector and the selector, the shift register receiving the shifting signals to activate the select signals;

a logic circuit including inputs connected to the shift register and the phase detector to receive the shifting signals and the select signal to provide coarse adjust signals; and

a controller connected to the logic circuit to receive the coarse adjust signals to adjust the coarse delay, wherein the coarse controller adjusts the coarse delay and the selector selects the fine delayed signal until the external and internal clock signals are synchronized.

14. The DLL of claim 13, wherein the delay line includes a plurality of delay stages, each of the delay stages includes a delay time, wherein each of the fine delay paths includes a delay time, wherein the delay time of each of the delay stages is greater than the delay time of each of the fine delay paths.

15. The DLL of claim 14, wherein the delay time of each of the delay stages is the same, wherein the delay time of each of the fine delay paths is not the same.

16. The DLL of claim 13, wherein a number of the fine delay paths is smaller than the number of the delay stages.

17. The DLL of claim 13, wherein the fine delay paths include a plurality of delay elements, wherein each of the delay element includes two inverters connected in series.

18. A memory device comprising:

a plurality of memory cells;

an output circuit connected to the memory cells; and

a delay locked loop (DLL) connected to the output circuit, the DLL comprising:

a coarse delay segment to apply a coarse delay to an external clock signal to generate a coarse delayed signal,

a fine delay segment connected to the coarse delay segment to apply a fine delay to the coarse delayed signal to generate an internal clock signal; and

wherein the fine delay segment is capable of adjusting the fine delay based on shifting signals that are generated when the external and internal signals are not synchronized, wherein the coarse delay is capable of adjusting the coarse delay based on the shifting signals and the fine delay applied to the coarse delay signal.

19. The memory device of claim 18, wherein each time the coarse delay segment adjusts the coarse delay, the fine delay segment changes the fine delay to a different amount of delay within a fine delay range of the fine delay segment.

20. The memory device of claim 18, wherein the output circuit receives the internal clock signal to capture a data signal from the memory cells during a memory operation,

21. The memory device of claim 18 further comprising a data bus, wherein the output circuit receives the internal clock signal to capture a data signal from the memory cells and outputs the data signal to the data bus during a memory operation, wherein the external clock signal and the data signal at the data bus are synchronized.

22. The memory device of claim 18, wherein the DLL further includes a model circuit, the model circuit being connected to the fine delay segment, wherein the model circuit is identical to the output circuit.

23. A memory device comprising:

a plurality of memory cells;

an output circuit connected to the memory cells; and

a delay locked loop (DLL) connected to the output circuit, the DLL comprising:

a coarse delay segment to apply a coarse delay to an external clock signal to generate a coarse delayed signal;

a fine delay segment connected to the coarse delay segment to apply a number of unequal amounts of fine delay to the coarse delayed signal to generate a plurality of fine delayed signals having different phase shifts,

a phase detector to generate shifting signals based on a difference in phase between the external and internal clock signals, wherein based on the shifting signals, the fine delay segment selects one of the fine delay signals to provide an internal clock signal; and

a logic circuit to receive the shifting signals and the select signal to enable the coarse delay segment to adjust the coarse delay.

24. The memory device of claim 23, wherein each time the coarse delay segment adjusts the coarse delay, the fine delay segment switches the internal clock signal between two fine delayed signals having unequal amounts of delay within a fine delay range.

25. The memory device of claim 23, wherein the output circuit receives the internal clock signal to capture a data signal from the memory cells during a memory operation.

26. The memory device of claim 23 further comprising a data bus, wherein the output circuit receives the internal clock signal to capture a data signal from the memory cells and outputs the data signal to the data bus during a memory operation, wherein the external clock signal and the data signal at the data bus are synchronized.

27. The memory device of claim 23, wherein the DLL further includes a model circuit, the model circuit being connected to the fine delay segment, wherein the model circuit is identical to the output circuit.

28. A system comprising:

a processor; and

a memory device connected to the processor, the memory device comprising:

a plurality of memory cells;

an output circuit connected to the memory cells;

a delay locked loop (DLL) connected to the output circuit, the DLL comprising:

a coarse delay segment to apply a coarse delay to an external clock signal to generate a coarse delayed signal;

a fine delay segment connected to the coarse delay segment to apply a fine delay to the coarse delayed signal to generate an internal clock signal; and

wherein the fine delay segment is capable of adjusting the fine delay based on shifting signals that are generated when the external and internal signals are not synchronized, wherein the coarse delay capable of adjusting the coarse delay based on the shifting signals and the fine delay applied to the coarse delay signal.

29. The system of claim 28, wherein each time the coarse delay segment adjusts the coarse delay, the fine delay segment changes the fine delay to a different amounts of delay within a fine delay range of the fine delay segment.

30. The system of claim 27 further comprising a data bus connected between the processor and the memory device, wherein the output circuit receives the internal clock signal to capture a data signal from the memory cells and outputs the data signal to the processor via the data bus during a memory operation, wherein the external clock signal and the data signal at the data bus are synchronized.

31. A system comprising:

a processor; and

a memory device connected to the processor, the memory device comprising:

a plurality of memory cells;

an output circuit connected to the memory cells;

a delay locked loop (DLL) connected to the output circuit, the DLL comprising:

a coarse delay segment to apply a coarse delay to an external clock signal to generate a coarse delayed signal;

a fine delay segment connected to the coarse delay segment to apply a number of unequal amounts of fine delay to the coarse delayed

signal to generate a plurality of fine delayed signals having different phase shifts,

a phase detector to generate shifting signals based on a difference in phase between the external and internal clock signals, wherein based on the shifting signals, the fine delay segment selects one of the fine delay signals to provide an internal clock signal; and

a logic circuit to receive the shifting signals and the select signal to enable the coarse delay segment to adjust the coarse delay.

32. The system of claim 31, wherein each time the coarse delay segment adjusts the coarse delay, the fine delay segment switches the internal clock signal between two fine delayed signals having unequal amounts of delay within a fine delay range.

33. The system of claim 31 further comprising a data bus connected between the processor and the memory device, wherein the output circuit receives the internal clock signal to capture a data signal from the memory cells and outputs the data signal to the processor via the data bus during a memory operation, wherein the external clock signal and the data signal at the data bus are synchronized.

34. A method of generating a clock signal, the method comprising:

delaying an external clock signal with a coarse delay to generate a coarse delayed signal;

applying a fine delay within a fine delay range to the coarse delayed signal to generate an internal clock signal;

generating shifting signals if the external and internal clock signals are not synchronized;

adjusting the fine delay based on the shifting signals; and

adjusting the coarse delay based on both the shifting signal and the fine delay being applied.

35. The method of claim 34 further includes comparing the external and internal clock signals to generate the shifting signals.

36. The method of claim 34, wherein applying a coarse delay includes applying a coarse delay within a coarse delay range, wherein the fine delay range is smaller than the coarse delay range.

37. The method of claim 34, wherein applying a coarse delay includes applying a coarse delay within a coarse delay range, wherein a maximum delay of the fine delay range is smaller than a minimum delay of the coarse delay range.

38. The method of claim 34, wherein adjusting the fine delay includes applying a different amount of fine delay within the fine delay range, wherein a largest amount of delay of the fine delay range is smaller than a smallest amount delay of a coarse delay range of the coarse delay segment.

39. The method of claim 34, wherein adjusting the coarse delay includes changing the fine delay between different amounts of delay of the fine delay range.

40. The method of claim 34, wherein adjusting the coarse delay includes increasing the coarse delay only when the fine delay is equal to a largest amount of delay of the fine delay range and the shifting signals indicate an increase in delay is necessary.

41. The method of claim 34, wherein adjusting the coarse delay includes decreasing the coarse delay only when the fine delay is equal to a smallest amount delay of the fine delay range and the shifting signals indicate a decrease in delay is necessary.

42. A method of generating a clock signal, the method comprising:

applying a coarse delay within coarse delay range to an external clock signal to generate a coarse delayed signal;

applying unequal amounts of fine delay within a fine delay range to the coarse delayed signal to generate a plurality of fine delayed signals;

selecting one of the fine delay signals to be an internal clock signal;

generating shifting signals based on a difference in phase between the external and internal clock signals; and

adjusting the coarse delay and fine delay in response to the shifting signals, wherein adjusting the coarse delay is based on the unequal amounts of fine delay applied to the coarse delayed signal.

43. The method of claim 42, wherein applying a coarse delay includes applying a coarse delay within a coarse delay range, wherein the fine delay range is smaller than the coarse delay range.

44. The method of claim 42, wherein selecting a fine delayed signal includes activating a select signal based on the shifting signal to select one of the fine signals.